Ameba-Z II

SINGLE-CHIP 802.11b/g/n 1T1R WLAN + Bluetooth SoC

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com

USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	**2018/09/13**	**Initial draft**
0.2	**2018/12/17**	**Swap pin 15, 16, and 17 for QFN40 CX/CF/CM packages**
0.3	**2018/12/25**	**Add section 2.2 & electrical characteristics**
0.4	**2019/1/4**	**Refine the features table**
0.5	**2019/1/17**	**Add part number RTL8720CN**
0.6	**2019/2/27**	**Add part number RTL8710CM-VA1**
0.7	**2019/3/28**	**Refine section 1.3.6 & section 4**
0.8	**2019/4/24**	**Refine section 1**

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1. Product Overview

1.1. General Description

Realtek Ameba-Z II series are highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controllers. It combines a KM4 MCU, WLAN MAC, a 1T1R capable WLAN baseband, RF, and Bluetooth in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

Ameba-Z II series integrate internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

1.2. Features

Table 1 Features of Ameba-Z II

Feature list			*RTL8720CF-VA1*	*RTL8720CM-VA1*	*RTL8720CN-VA1*
Package			QFN40	QFN40	QFN40
Dimension			5x5 mm^2	5x5 mm^2	5x5 mm^2
CPU	Core type		KM4	KM4	KM4
	Max. core clock		100MHz	100MHz	100MHz
Memory	Internal ROM		384KB	384KB	384KB
	Internal SRAM		256KB	256KB	256KB
	Flash		2MB	No	No
	pSRAM		No	4MB	No
SWD/JTAG			SWD/JTAG	SWD/JTAG	SWD/JTAG
WIFI	802.11 b/g/n		Yes	Yes	Yes
BT Config			Yes	Yes	Yes
Peripherals	UART		3	3	3
	SPI Master	Max. 20Mbps	1	1	1
	SPI Slave	Max. 4Mbps	1	1	1
	I2C	Max. 400Kbps	1	1	1
	GDMA	2 channel	1	1	1
	GPIO	IN/OUT/INT	20	16	16
	Timer	Basic timer use 32K	1	1	1

		Advanced timer use 40M	8	8	8
	PWM	Output	8	8	8
	WDG		1	1	1
	SDIO 2.0 Device		1	1	1
External 32K			1	1	1
Dsleep Wakepin	Deep sleep wake pin		20	16	16

NOTE: The number of GPIO pins is assumed that external flash operates in dual I/O mode.

1.3. Package Types and Pin Descriptions

1.3.1. RTL8720CF-VA1 (QFN40)

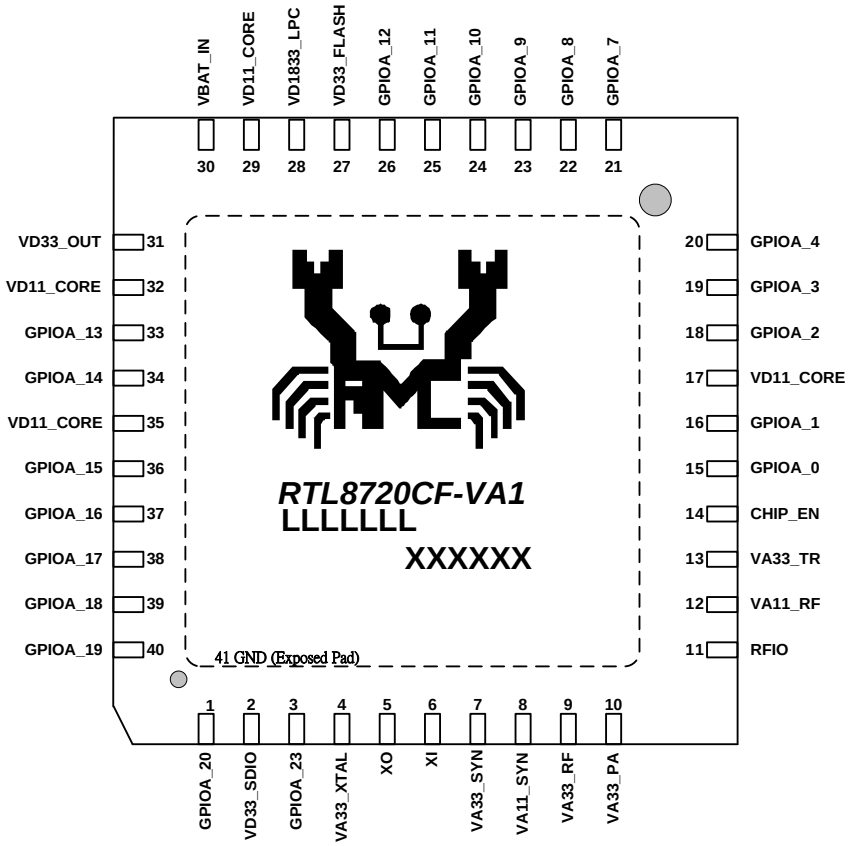

Figure 1 RTL8720CF-VA1 QFN40 Pin Assignments

1.3.2. RTL8720CM-VA1 (QFN40)

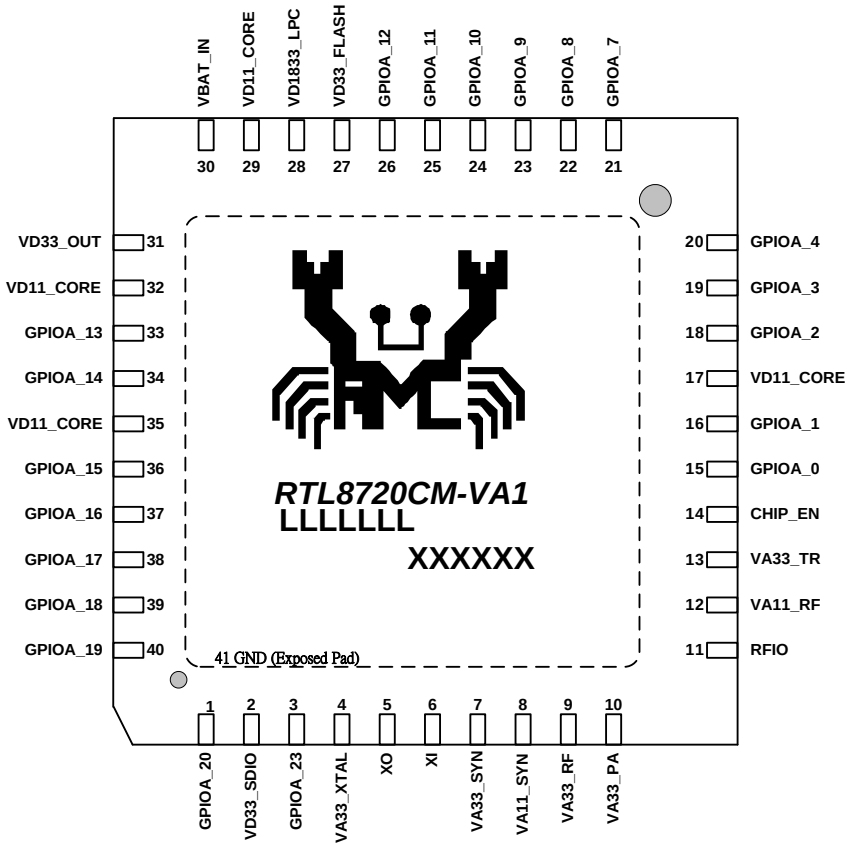

Figure 2 RTL8720CM-VA1 QFN40 Pin Assignments

1.3.3. RTL8720CN-VA1 (QFN40)

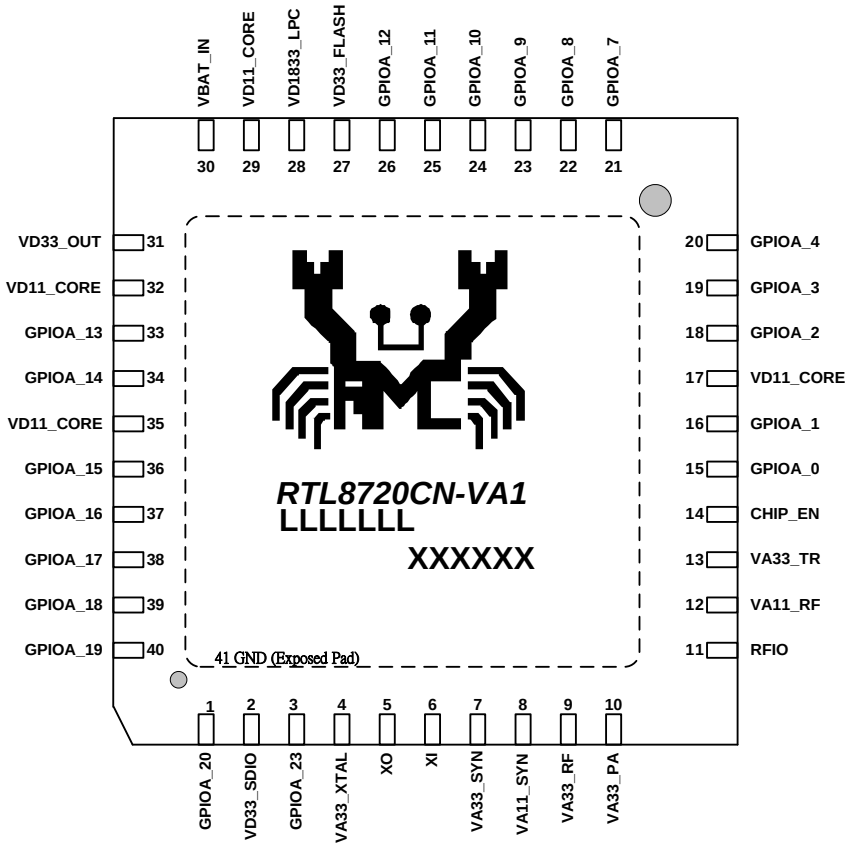

Figure 3 RTL8720CN-VA1 QFN40 Pin Assignments

1.3.4. Pin Descriptions

The following signal type codes are used in the tables:

Table 2 Pin Description

I:	*Input*	*O:*	*Output*
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin

1.3.4.1 Power On Trap Pin

Table 3 Power On Trap Pins

Symbol	*Type*	*RTL8720CF-VA1*	*RTL8720CM-VA1*	*RTL8720CN-VA1*	*Description*
TEST_MODE_SEL	I	15	15	15	Shared with GPIOA_0 1: Enter into test/debug mode 0: Normal operation mode
Autoload_Fail	I	16	16	16	Shared with GPIOA_1 1: eFUSE settings are not loaded 0: eFUSE settings are loaded
SPS_LDO_SEL	I	3	3	3	Shared with GPIOA_23 1: LDO 0: SWR

1.3.4.2 RF pin

Table 4 RF pin

Symbol	*Type*	*RTL8720CF-VA1*	*RTL8720CM-VA1*	*RTL8720CN-VA1*	*Description*
RF_IO	IO	11	11	11	WL RF signal

1.3.4.3 CHIP EN

Table 5 CHIP EN

Symbol	Type	RTL8720CF-VA1	RTL8720CM-VA1	RTL8720CN-VA1	Description
CHIP_EN	I	14	14	14	Enable chip. 1: enable chip; 0: shutdown chip

1.3.4.4 Power Pins

Table 6 Power Pins

Symbol	Type	RTL8720CF-VA1	RTL8720CM-VA1	RTL8720CN-VA1	Description
VD33_SDIO	P	2	2	2	Power source for I/O power, 3.3V±10%
VA33_XTAL	P	4	4	4	Power source for Analog Circuit, 3.3V±10%
VA33_SYN	P	7	7	7	Power source for Analog Circuit, 3.3V±10%
VA11_SYN	P	8	8	8	Power source for Analog Circuit, 1.1V±5%
VA33_RF	P	9	9	9	Power source for Analog Circuit, 3.3V±10%
VA33_PA	P	10	10	10	Power source for Analog Circuit, 3.3V±10%
VA11_RF	P	12	12	12	Power source for Analog Circuit, 1.1V±5%
VA33_TR	P	13	13	13	Power source for Analog Circuit, 3.3V±10%
VD11_CORE	P	17	17	17	Power source for the core, 1.1V±5%
VD33_FLASH	P	27	27	27	Power source for I/O power, 3.3V±10%
VD1833_LPC	P	28	28	28	3.3V±10% for RTL8720CF-VA1 and RTL8720CN-VA1 1.8V for RTL8720CM-VA1
VD11_CORE	P	29	29	29	Power source for the core, 1.1V±5%

VBAT_IN	P	30	30	30	5V±10% input or 3.3V±10% input
VD33_OUT	P	31	31	31	(1) 3.3V output from LDO (when PIN 30 *VBAT_IN* is 5V input) (2) 3.3V±10% input (when PIN 30 *VBAT_IN* is 3.3V input)
VD11_CORE	P	32	32	32	1.1V output from SWR/LDO
VD11_CORE	P	35	35	35	Power source for the core, 1.1V±5%

1.3.4.5 XTAL Pins

Table 7 XTAL Pins

Symbol	*Type*	*RTL8720CF-VA1*	*RTL8720CM-VA1*	*RTL8720CN-VA1*	*Description*
XI	I	6	6	6	Input of 40MHz Crystal Clock Reference
XO	O	5	5	5	Output of 40MHz Crystal Clock Reference

1.3.4.6 GPIO Pins

Table 8 GPIO pins

Symbol	*Type*	*RTL8720CF-VA1*	*RTL8720CM-VA1*	*RTL8720CN-VA1*	*Description*
GPIOA_20	I/O	1	1	1	SD_D1
					SPI_M_D1
					UART2_RTS
					SPI_MISO
					I2C_SDA
					PWM0
GPIOA_23	I/O	3	3	3	LED0
					PWM7
GPIOA_0	I/O	15	15	15	JTAG_CLK
					UART1_IN

					EXT_32K
					PWM0
GPIOA_1	I/O	16	16	16	JTAG_TMS
					UART1_OUT
					PWM1
GPIOA_2	I/O	18	18	18	JTAG_TDO
					UART1_IN
					SPI_CS
					I2C_SCL
					PWM2
GPIOA_3	I/O	19	19	19	JTAG_TDI
					UART1_OUT
					SPI_SCL
					I2C_SDA
					PWM3
GPIOA_4	I/O	20	20	20	JTAG_TRST
					UART1_CTS
					SPI_MOSI
					PWM4
GPIOA_7	I/O	21	21	21	SPI_M_CS
					SPI_CS
GPIOA_8	I/O	22	22	22	SPI_M_CLK
					SPI_SCL
GPIOA_9	I/O	23	23	23	SPI_M_D2
					UART0_RTS
					SPI_MOSI
GPIOA_10	I/O	24	24	24	SPI_M_D1
					UART0_CTS
					SPI_MISO
GPIOA_11	I/O	25	25	25	SPI_M_D0
					UART0_OUT

					I2C_SCL
					PWM0
GPIOA_12	I/O	26	26	26	SPI_M_D3
					UART0_IN
					I2C_SDA
					PWM1
GPIOA_13	I/O	33	33	33	UART0_IN
					PWM7
GPIOA_14	I/O	34	34	34	SDIO_INT
					UART0_OUT
					PWM2
GPIOA_15	I/O	36	36	36	SD_D2
					SPI_M_CS
					UART2_IN
					SPI_CS
					I2C_SCL
					PWM3
GPIOA_16	I/O	37	37	37	SD_D3
					SPI_M_CLK
					UART2_OUT
					SPI_SCL
					I2C_SDA
					PWM4
GPIOA_17	I/O	38	38	38	SD_CMD
					SPI_M_D2
					PWM5
GPIOA_18	I/O	39	39	39	SD_CLK
					SPI_M_D3
					PWM6
GPIOA_19	I/O	40	40	40	SD_D0
					SPI_M_D0

					UART2_CTS
					SPI_MOSI
					I2C_SCL
					PWM7

2. Block Diagram

2.1. Functional Block Diagram

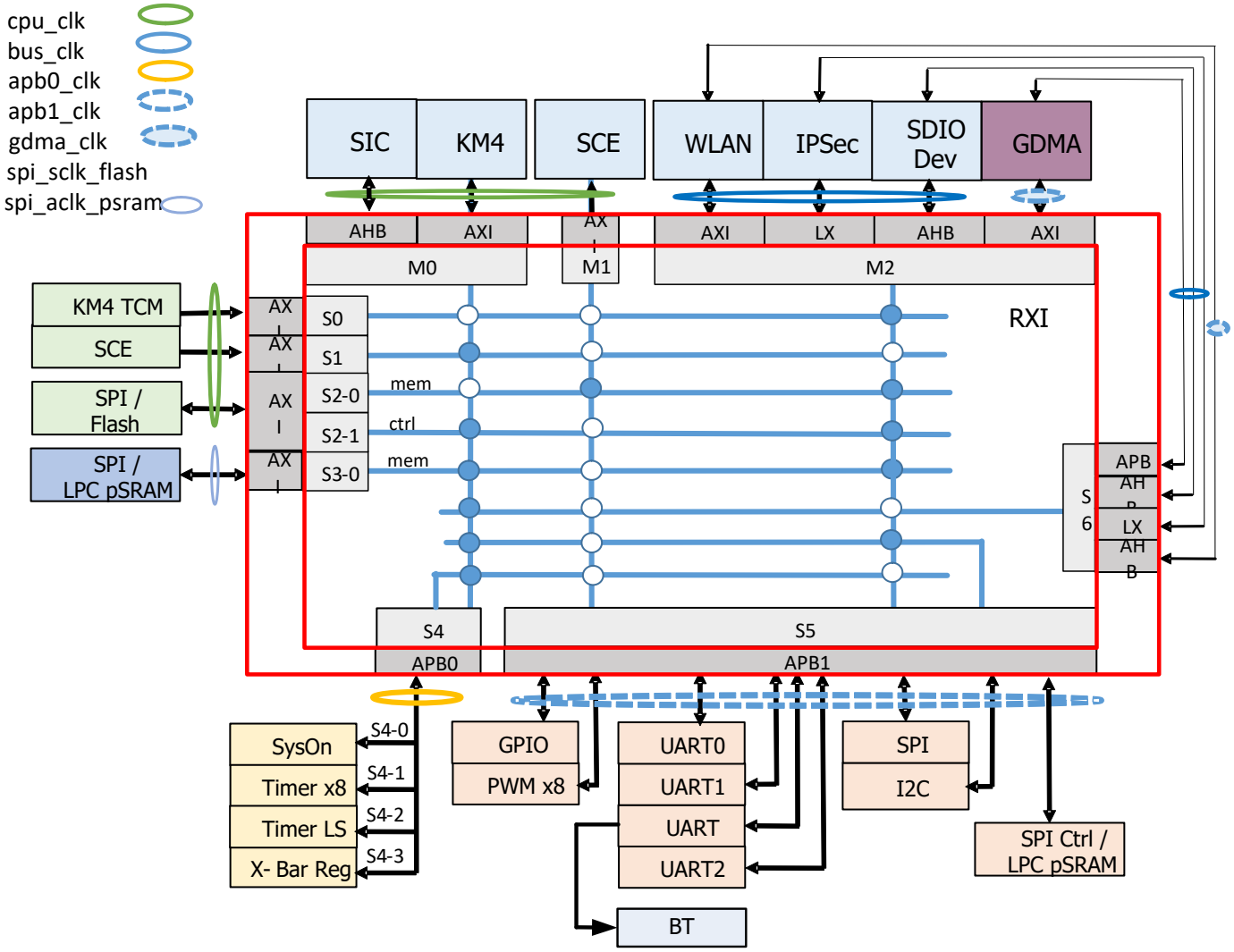

Figure 4 Block Diagram

2.2. Power Supply Application Diagram

According to different power source, the power architecture can have two types:

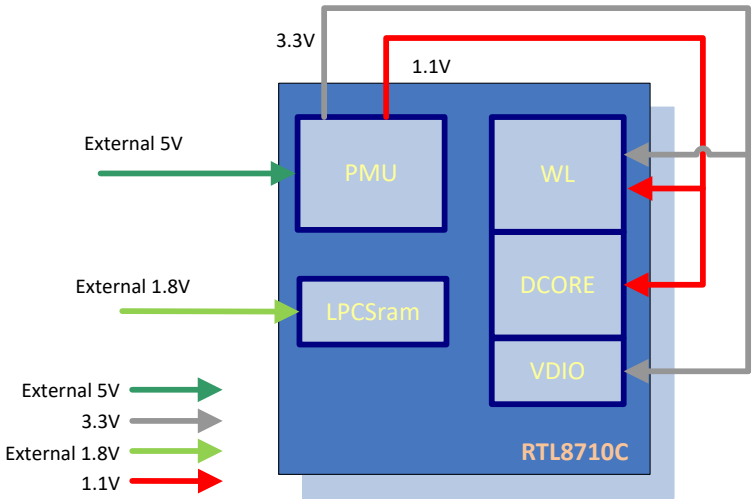

Figure 5 5V Power Supply Architecture

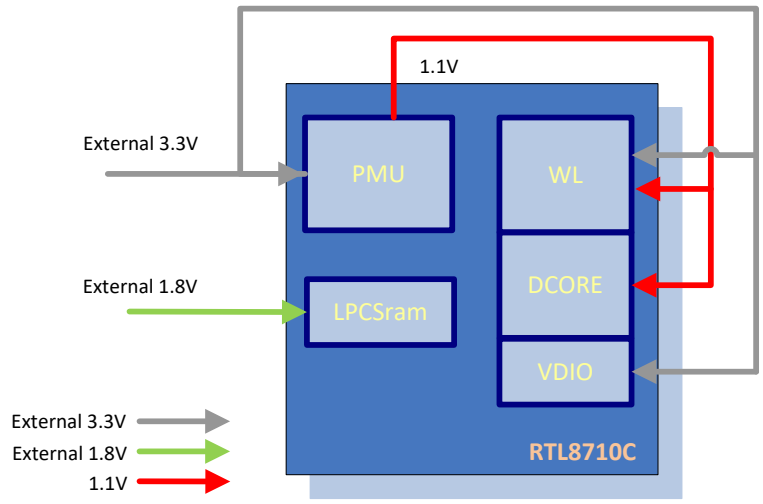

Figure 6 3.3V Power Supply Architecture

3. Memory Mapping

3.1. Programming Space

Table 9 Programming Space

Secure Attribute	*Cache*	*Start Address*	*Size*	*IP Function*
Configurable	X	0x0000_0000	384KB	ITCM ROM
Configurable	X	0x1000_0000	256KB	ITCM SRAM
Non-Secure	V	0x2000_0000	32KB	Additional SRAM (for CPU access only, H/W buffer usage is prohibited)

3.2. IO Space

Table 10 IO Space

Secure Attribute	*Cache*	*Start Address*	*Size*	*IP Function*
Non-Secure	X	0x4000_0000	2KB	SYS Control (SYSON)
Non-Secure	X	0x4000_1000	2KB	GPIO
Non-Secure	X	0x4000_1C00	1KB	PWM Control
Non-Secure	X	0x4000_2000	4KB	Timer
Non-Secure	X	0x4000_3000	1KB	UART0
Non-Secure	X	0x4000_3800	2KB	Timer LS
Non-Secure	X	0x4000_4000	8KB	Cross-Bar Control register (NS)
Non-Secure	X	0x4002_0000	4KB	SPI flash controller
Non-Secure	X	0x4004_0000	1KB	UART1
Non-Secure	X	0x4004_0400	1KB	UART2
Non-Secure	X	0x4004_2000	1KB	SPI
Non-Secure	X	0x4004_4000	1KB	I2C
Non-Secure	X	0x4005_0000	16KB	SDIO Device
Non-Secure	X	0x4006_0000	2KB	GDMA
Non-Secure	X	0x4007_0000	16KB	IPSec
Non-Secure	X	0x4008_0000	256KB	WLAN REG & TX/RX FIFO direct map

Non-Secure	X	0x4060_0000	4KB	spic_ctl_psram
Secure	X	0x5000_0800	2KB	SYS Control (SYSON)
Secure	X	0x5000_2000	4KB	Timer
Secure	X	0x5000_4000	8KB	Cross-Bar Control register
Secure	X	0x5006_0000	2KB	GDMA
Secure	X	0x5007_0000	16KB	IPSec

3.3. Extension Memory Space

Table 11 Extension Memory Space

Secure Attribute	*Cache*	*Start Address*	*Size*	*IP Function*
Configurable	V	0x9800_0000	128MB	External flash memory

3.4. Internal ROM

384KB ROM is integrated to provide high access speed, low leakage memory. The ROM memory clock speed is up to 100MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Peripheral Drivers & API
- Non-flash booting functions and drivers
- Security function libs

3.5. Internal SRAM

Max. 256KB SRAM is integrated to provide instruction, data, and buffer usage. The maximum clock speed is up to 100MHz.

CHIP	*RTL8720CF-VA1*	*RTL8720CM-VA1*	*RTL8720CN-VA1*
SRAM	256KB	256KB	256KB

3.6. SPI NOR Flash

3.6.1. Features

- SPI baud rate:
  - 50/33/25/20MHz …
- Execute in place (XIP):
  - we supports a memory-mapped I/O interface for read operation
  - Support 32K I/D read cache, 2-way associative
  - Support decryption on the fly
- SPI mode:
  - SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI
- Flash size
  - Support up to 128MB flash size

4. Pin Function Table

Table 12 Pin Function Table

Pin Name	SPIC-Flash/SDIO	JTAG	UART	SPI/WL_LED/EXT_32K	I2C	PWM
GPIOA_0		JTAG_CLK	UART1_IN	EXT_32K		PWM[0]
GPIOA_1		JTAG_TMS	UART1_OUT	BT_LED		PWM[1]
GPIOA_2		JTAG_TDO	UART1_IN	SPI_CSn	I2C_SCL	PWM[2]
GPIOA_3		JTAG_TDI	UART1_OUT	SPI_SCL	I2C_SDA	PWM[3]
GPIOA_4		JTAG_TRST	UART1_CTS	SPI_MOSI		PWM[4]
GPIOA_7	SPI_M_CS			SPI_CSn		
GPIOA_8	SPI_M_CLK			SPI_SCL		
GPIOA_9	SPI_M_DATA[2]		UART0_RTS	SPI_MOSI		
GPIOA_10	SPI_M_DATA[1]		UART0_CTS	SPI_MISO		
GPIOA_11	SPI_M_DATA[0]		UART0_OUT		I2C_SCL	PWM[0]
GPIOA_12	SPI_M_DATA[3]		UART0_IN		I2C_SDA	PWM[1]
GPIOA_13			UART0_IN			PWM[7]
GPIOA_14	SDIO_INT		UART0_OUT			PWM[2]
GPIOA_15	SD_D[2]		UART2_IN	SPI_CSn	I2C_SCL	PWM[3]
GPIOA_16	SD_D[3]		UART2_OUT	SPI_SCL	I2C_SDA	PWM[4]
GPIOA_17	SD_CMD					PWM[5]
GPIOA_18	SD_CLK					PWM[6]
GPIOA_19	SD_D[0]		UART2_CTS	SPI_MOSI	I2C_SCL	PWM[7]
GPIOA_20	SD_D[1]		UART2_RTS	SPI_MISO	I2C_SDA	PWM[0]
GPIOA_23				LED_0		PWM[7]

5. Power Management Control Unit

5.1. Power Mode and Power Consumption

Table 13 Power Consumption

Power Mode	*Power Consumption*		
	Typical	*Maximum*	*Units*
Deep Sleep Mode	TBD	TBD	uA
Deep Standby Mode	TBD	TBD	uA

5.2. Shutdown Mode

CHIP_EN deasserts to shutdown whole chip without external power cut components required.

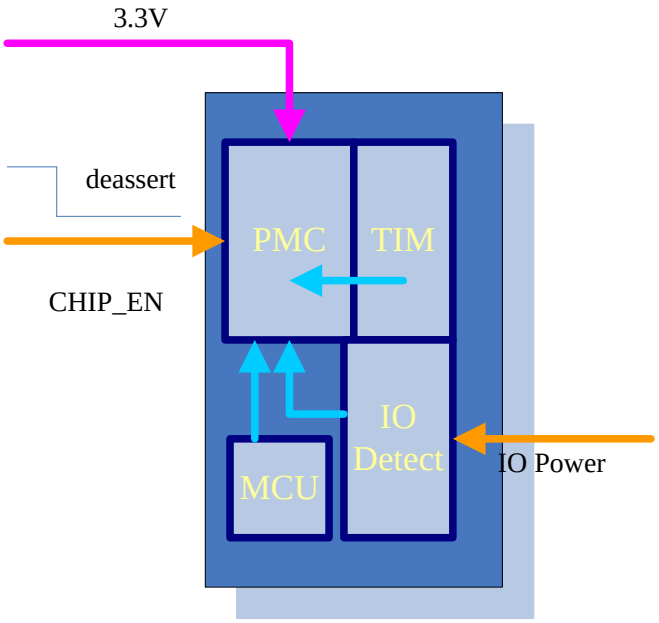

Figure 7 Shutdown Mode

5.3. Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API.

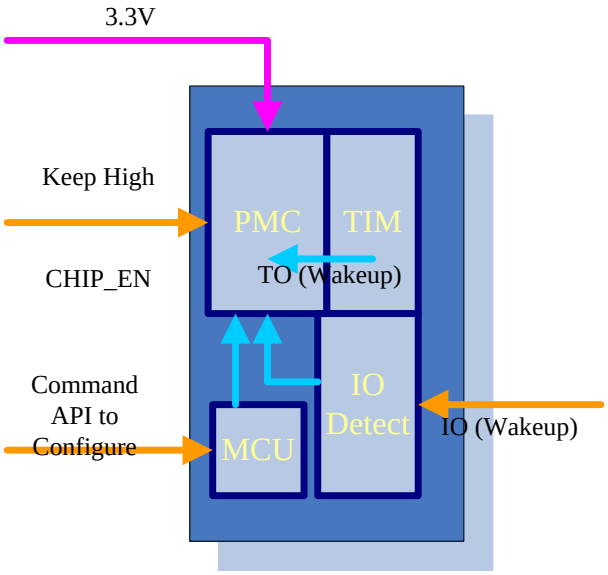

Figure 8 Deep Sleep Mode

5.3.1. Power Domain

Table 14 Deep Sleep Mode Power Domain

Functions	*Power State*	*Comment*
KM4 core	OFF	
system clock	OFF	
SRAM	OFF	
Regulator	OFF	
Peripherals	OFF	
low precision timer	ON	1
Dsleep wake pin	ON	20 or 14 (depend on package)

5.3.2. Wakeup Source

Table 15 Deep Sleep Mode Wakeup Source

Wakeup source	*Wakeup*	*Comment*
low precision timer	YES	
Dsleep Wake pin	YES	GPIOA_0 GPIOA_1 GPIOA_2 GPIOA_3 GPIOA_4 GPIOA_7 GPIOA_8 GPIOA_9 GPIOA_10 GPIOA_11 GPIOA_12 GPIOA_13 GPIOA_14 GPIOA_15 GPIOA_16 GPIOA_17 GPIOA_18 GPIOA_19 GPIOA_20 GPIOA_23

5.4. Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API.

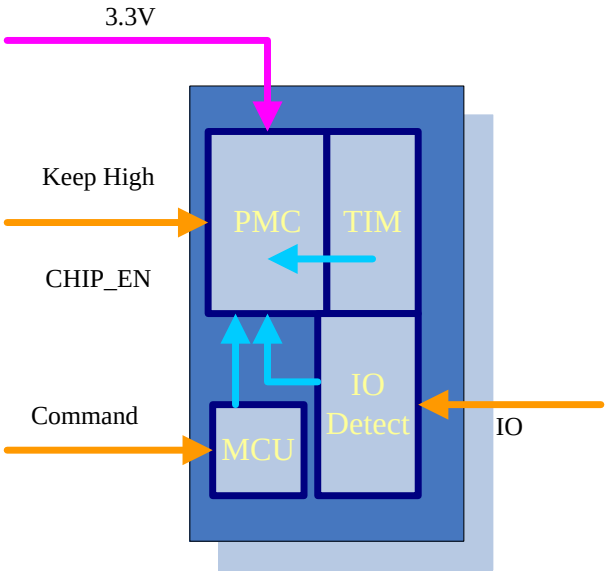

Figure 9 Deep Standby Mode

5.4.1. Power Domain

Table 16 Deep Standby Mode Power Domain

functions	*Power State*	*comment*
KM4 core	OFF	
system clock	OFF	
SRAM	OFF	
Regulator	OFF	
Peripherals	OFF	
System timer	ON	1
low precision timer	ON	1
wake pin	ON	20 or 14 (depend on package)

5.4.2. Wakeup Source

Table 17 Deep Standby Mode Wakeup Source

Wakeup source	*Wakeup*	*Comment*
Wake pin	YES	GPIOA_0 GPIOA_1 GPIOA_2 GPIOA_3 GPIOA_4 GPIOA_7 (depend on package) GPIOA_8 (depend on package) GPIOA_9 (depend on package) GPIOA_10 (depend on package) GPIOA_11 (depend on package) GPIOA_12 (depend on package) GPIOA_13 GPIOA_14 GPIOA_15 GPIOA_16 GPIOA_17 GPIOA_18 GPIOA_19 GPIOA_20 GPIOA_23
System timer	YES	
low precision timer	YES	

6. General Purpose Timer

6.1. Features of GTimer

- 8 Gtimer supported at HS domain and 1 Gtimer supported at LP domain
- The source clock of the HS Gtimer is from 40MHz
- The source clock of the LP Gtimer is from 32KHz
- Support Counter mode and timer mode
- Each Gtimer support 4 match event

7. PWM Interface

7.1. Features of PWM

- Support maximum 8 PWM functions
- 0~100% duty can be configurable
- Use selected HS Gtimer interrupt as counter source
- Minimum resolution is 50ns
- The period can be configured up to 8 seconds

8. UART

8.1. Application scenario

The Ameba-Z II series UART is basically used for serial communication with a peripheral, modem (data carrier equipment, or data set). For IOT devices, the power consumption is the most important consideration, so there is an advanced hardware which called RX-Filter built in Ameba-Z II series UART. It is designed to filter RX data, and then wake up the CPU from sleep mode when the RX data is matching with wakeup condition. By this way, the CPU will be waked up only when needed.

8.2. Feature List

- Support maximum 3 x UART with 40 MHz clock source (maximum baud rate 4M Hz)
- UART (RS232 Standard) Serial Data Format
- Programmable Asynchronous Clock Support
- 16 bytes Transmit Data FIFO and 32 bytes Receive Data FIFO
- Programmable Receive Data FIFO Trigger Level
- DMA data moving support to save MCU loading
- Programmable RX Filter
- Auto flow control

8.3. Architecture

The UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. Users basically can set TX data or get RX data from Transmitter Holding Register/Receiver Buffer Register. To set or get more information of TX/RX FIFO via accessing FIFO Control registers. In order to generate the desired baud rate and data format, users can access configuration registers which are related to line control information and Baud rate setting parameters. There are also GDMA channels for UART TX/RX mode transfer.

For some applications, the system can be waked up from sleep mode by receiving a packet with special characters ahead. To reduce the power consumption of the system when it is in sleep mode, the RX filter hardware is designed to check the first 1 or 2 bytes of a packet from the UART receiving. So the CPU does not need to be waked up to check every received UART byte. The CPU will be waked up only when an ‘interested’ packet is received.

In order to support high and low speed baud rate, the Ameba-Z II series provides multiple UART clocks. The default baud rate is 115.2k.

Desired Baud Rate	Actual Baud Rate	Error(%)
110	110.0533759	0.048523534
300	300.120048	0.040016006
600	600.240096	0.040016006
1200	1200.480192	0.040016006
2400	2400.960384	0.040016006
4800	4801.920768	0.040016006
9600	9603.841537	0.040016006
14400	14414.41441	0.1001001
19200	19230.76923	0.16025641
28800	28860.02886	0.208433542
38400	38461.53846	0.16025641
57600	57720.05772	0.208433542
76800	76923.07692	0.16025641
115200	115243.583	0.037832489
128000	128205.1282	0.16025641
153600	153846.1538	0.16025641
230400	231092.437	0.300536881

Desired Baud Rate	Actual Baud Rate	Error(%)
380400	380952.381	0.145210555
460800	460732.9843	0.014543339
500000	500000	0
921600	922431.8658	0.090263219
1000000	1000000	0
1382400	1383647.799	0.090263219
1444400	1452145.215	0.536223658
1500000	1506849.315	0.456621005
1843200	1856540.084	0.723745898
2000000	2000000	0
2100000	2105263.158	0.250626566
2764800	2784810.127	0.723745898
3000000	3013698.63	0.456621005
3250000	3283582.09	1.033295063
3692300	3728813.559	0.988910959
3750000	3793103.448	1.149425287
4000000	4000000	0

9. SPI Interface

9.1. Features of SPI

- Support one SPI port
- Support three interfaces
  - Motorola Serial Peripheral Interface (SPI)
  - Texas Instruments Serial Protocol (SSP)
  - National Semiconductor Microwire
- SPI device can be configured as a SPI master or a SPI slave
- Maximum speed support for each SPI interface is listed below

	Master	Slave
SPI 0	20 MHz	5 MHz (Receive only) 4 MHz (Transmit/Receive)

- Support DMA handshaking interface to enable DMA transfer with SPI
- Support 8 bit and 16 bit data frame size
- Programmable clock polarity and clock phase for SPI interface

	SCPOL = 0	**SCPOL = 1**
SCPH = 0	Mode 0	Mode 2
SCPH = 1	Mode 1	Mode 3

- Support bit swapping and byte swapping features
- The depth of transmit FIFO and receive FIFO are 1024 bit
  - 64 data frames at most

10. I2C Interface

10.1. Features of I2C

- Two speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (< 400 Kb/s)
- Master or Slave I2C operation
- 7- or 10-bit addressing
- Interrupt or polled mode operation
- TX and RX DMA support

11. General Purpose DMA Controller

11.1. Features of GDMA

- One port DMA with totally 2 channels
- Two channels can be configured independently and can transfer data concurrently.
- Configurable endian
- Support memory-memory, memory-peripheral and peripheral-memory DMA transfer
- Support secure transaction under secure domain

12. SDIO/RTK SPI Device Mode Interface

12.1. Features of SDIO/RTK SPI Device Mode Interface

- Support SDIO 2.0 High Speed mode
- CIS can be configured with internal non-volatile memory for fast card detection
- RTK SPI provides high efficiency SPI interface with interrupt and full duplex mode
- Support high performance Ethernet to WIFI transformation
- Support non-flash booting in the use of Ethernet to WIFI transformation card

12.2. SDIO Device Mode Specifications

12.2.1. Bus Timing Specification

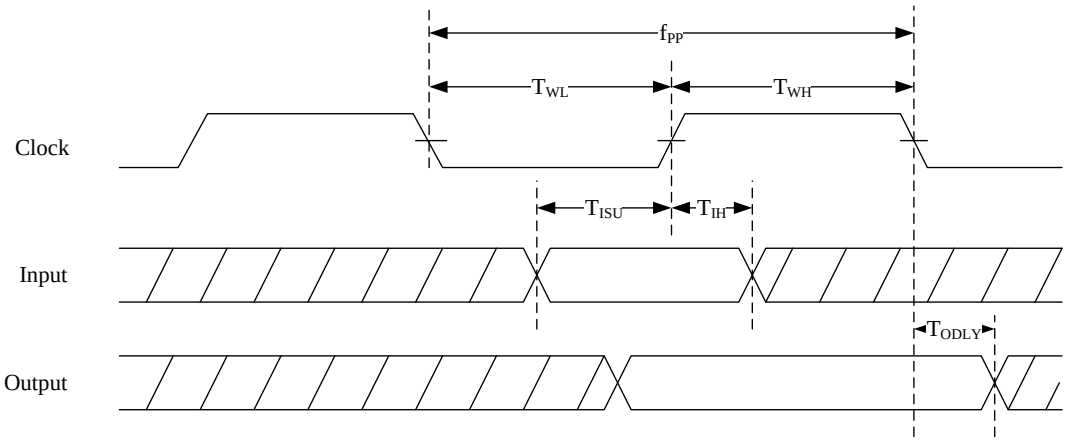

Table 18 SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	**Clock Frequency**	**Default**	**0**	**25**	**MHz**
		HS	**0**	**50**	**MHz**
T_{WL}	**Clock Low Time**	**DEF**	**10**	**-**	**ns**
		HS	**7**	**-**	**ns**
T_{WH}	**Clock High Time**	**DEF**	**10**	**-**	**ns**
		HS	**7**	**-**	**ns**
T_{ISU}	**Input Setup Time**	**DEF**	**5**	**-**	**ns**

NO	Parameter	Mode	MIN	MAX	Unit
		HS	**6**	**-**	**ns**
T_{IH}	**Input Hold Time**	**DEF**	**5**	**-**	**ns**
		HS	**2**	**-**	**ns**
T_{ODLY}	**Output Delay Time**	**DEF**	**-**	**14**	**ns**
		HS	**-**	**14**	**ns**

13. GPIO Functions

13.1. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

14. Security Engine

14.1. Application scenario

The Ameba-Z II series security engine provides low SW computing and high performance cryptographic operation (such as authentication, encryption and decryption). In other words, it's more secure, faster and saves more CPU and Memory resources than software cryptographic operation.

14.2. Feature list

- Supported authentication algorithms:
  - MD5
  - SHA-1
  - SHA-2 (SHA-224 / SHA-256)
  - HMAC-MD5
  - HMAC-SHA1
  - HMAC-SHA2 (SHA-224 / SHA-256)
- Supported Encryption / Decryption mechanisms:
  - AES-128 (CBC / ECB / CTR / CFB / OFB / GCTR / GCM)
  - AES-192 (CBC / ECB / CTR / CFB / OFB / GCTR / GCM)
  - AES-256 (CBC / ECB / CTR / CFB / OFB / GCTR / GCM)
- Supported programmable CRC

14.3. Architecture

Security engine implements many kinds of cryptographic operation. For users, the way of setting basic cryptographic operation parameters is writing data into Source/Destination descriptor registers. Source descriptor register is used to set input parameters (HMAC Key, Cipher Key, IV , AAD and Plaintext buffer); Destination descriptor register is used to set output parameters (Digest/Cipher result buffer). Users can disassemble a Source/Destination packet command into hardware FIFO in Source/Destination descriptors, then Packet-base arbiter will choose which FIFO node to DMA engine. However, this situation is only used in setting authentication or cipher operation parameters, because setting CRC operation parameters is different from them. If users want to set CRC operation parameters, just write data into the CRC control registers which are related to CRC in Non-Secure mode, because only Non-Secure mode supports CRC

registers.

DMA engine gets buffer address from the Source/Destination Descriptor FIFO node, then it access the address. It moves data into Security engine, after Security engine calculation, it will help move the result data to the result buffer.

15. WIFI

15.1. General

- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 65Mbps receive PHY rate and 65Mbps transmit PHY rate using 20MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

15.2. Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WIFI Direct support

15.3. WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism

15.4. WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz bandwidth transmission
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

- Maximum data rate 26Mbps in 802.11g and 65Mbps in 802.11n

16. Bluetooth

16.1. Application scenario

The RTL8720 series highly integrated Bluetooth Low Energy controller with a UART interface. It combines a BLE Protocol (PHY, LL, L2CAP, SM, ATT, GAP, GATT), BLE Baseband, Modem, and BLE RF in chip, also supports BLE user GATT-based profile application.

16.2. Features

- Bluetooth 4.2 Low Energy (F/W supported)

17. Electrical Characteristics

17.1. Temperature Limit Ratings

Table 19 Temperature Limit Ratings

Parameter	*Minimum*	*Maximum*	*Units*
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-20	+85	°C
Junction Temperature	0	+125	°C

17.2. Electrical Characteristics

Table 20 Power Supply DC Characteristics

Symbol	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Units*
IDD33	**3.3V Rating Current (with internal regulator and integrated CMOS PA)**	-	-	**450**	**mA**
IDD_IO	**IO Rating Current (including VDD_IO)**			**200**	**mA**
IRSH33	**3.3V Inrush current**	--	--	**800**	**mA**

17.3. Digital IO Pin DC Characteristics

17.3.1. Electrical Specifications

Table 21 Typical Digital IO DC Parameters

Symbol	*Parameter*	*Conditions*	*Min.*	*Typ.*	*Max.*	*Units*	*Note*
V_{IH}	**Input-High Voltage**	**LVTTL**	**2.0**	-	-	**V**	
V_{IL}	**Input-Low Voltage**	**LVTTL**	-	-	**0.8**	**V**	
V_{OH}	**Output-High Voltage**	**LVTTL**	**2.4**	-	-	**V**	
V_{OL}	**Output-Low Voltage**	**LVTTL**	-	-	**0.4**	**V**	
V_{T+}	**Schmitt-trigger High Level**		**1.377**	**1.683**	**1.908**	**V**	
V_{T-}	**Schmitt-trigger Low Level**		**0.729**	**0.957**	**1.116**	**V**	
I_{IL}	**Input-Leakage Current**	V_{IN}**=3.3V or 0**	**-10**	**±1**	**10**	**μA**	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Note
R_{PU}	Input Pull-Up Resistance			75		KΩ	
R_{PD}	Input Pull-Down Resistance			75		KΩ	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.

17.4. Power State and Power Sequence

17.4.1. Power On Sequence

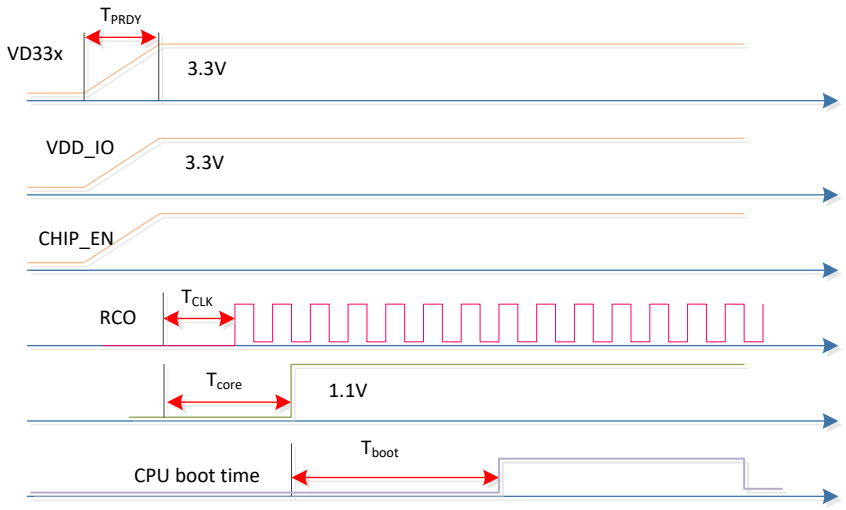

Figure 10 Power-On Sequence

Symbol	Parameter	Minimum	Typical	Maximum	Unit
TPRDY	3.3V ready time	0.6	0.6	1	ms
T_{CLK}	Internal ring clock stable time after 3.3V ready	1			ms
T_{core}	Core power ready time	1.5	1.5		ms
T_{boot}	Application ready time				ms
V_{RST}	Shutdown occurs after CHIP_EN lower than this voltage	0	0	1.65	V
T_{RST}	The require time that CHIP_EN lower than V_{RST}	--	10	--	us

17.4.2. Resume from Standby

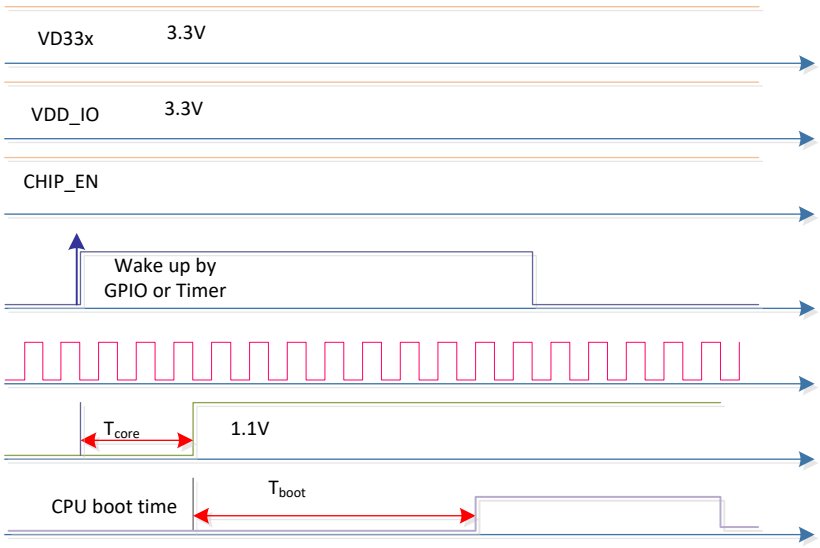

Figure 11 Timing Sequence of Resume from Standby

17.4.3. Shutdown Sequence

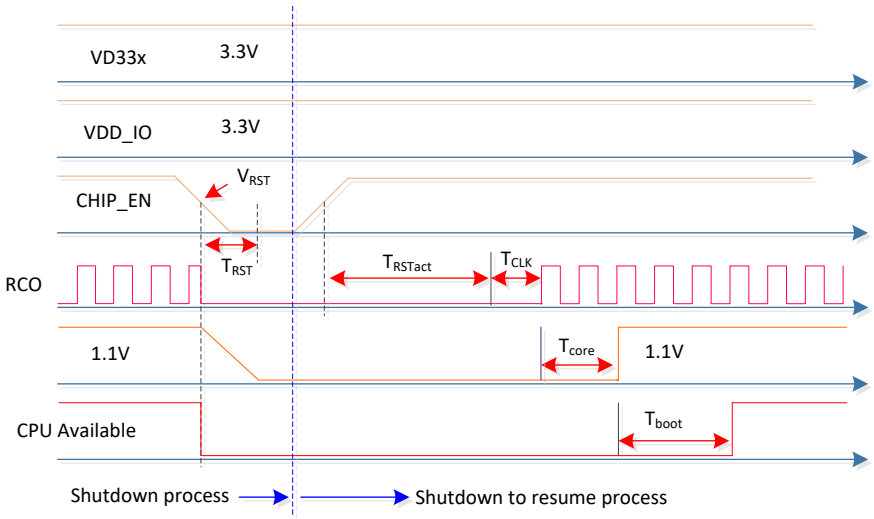

Figure 12 Timing Sequence of Shutdown

18. Mechanical Dimensions

18.1. Package Specification

18.1.1. QFN40

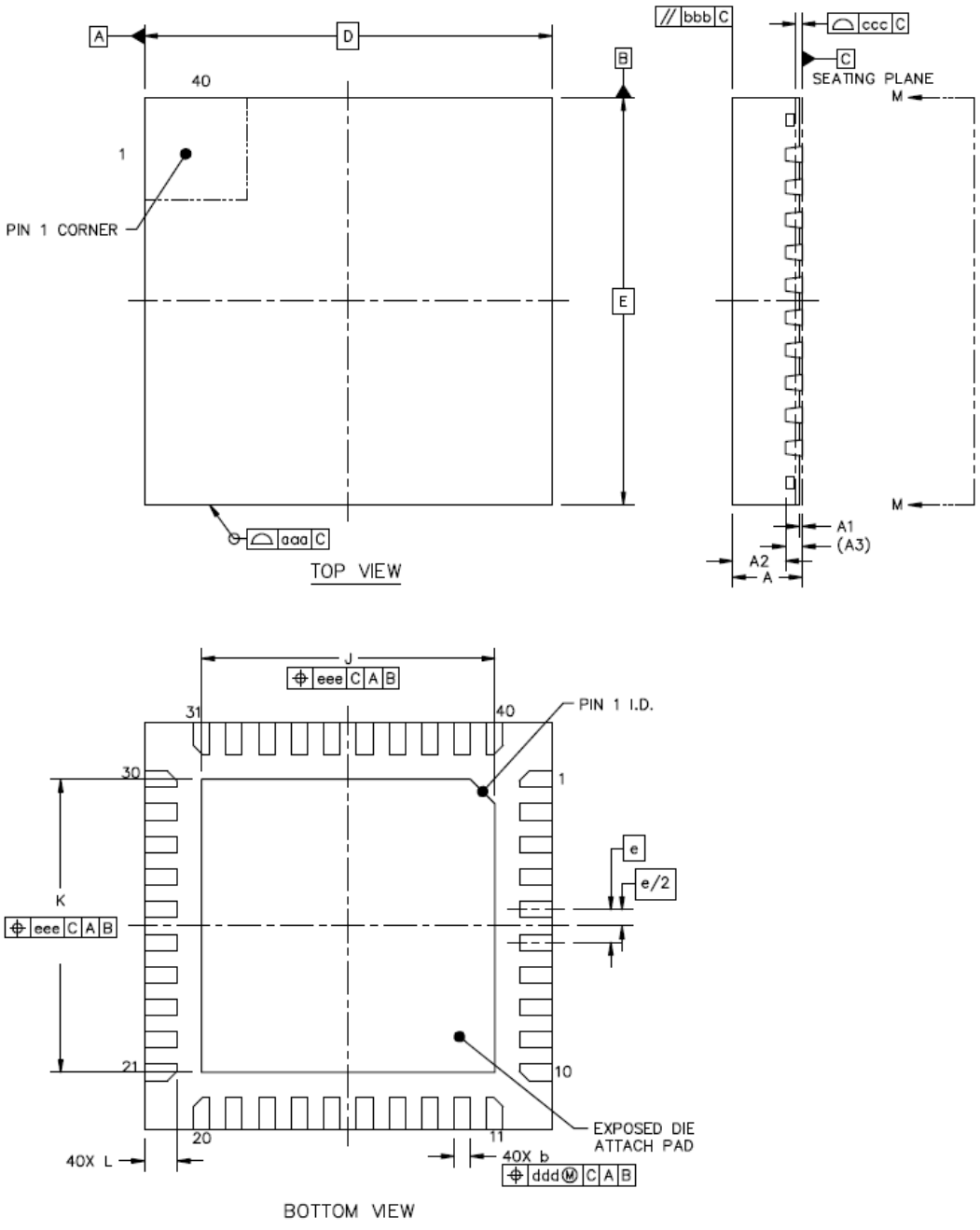

Figure 13 QFN40 Package Specification

Table 22 QFN40 Package Specification

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	0.67
A3	0.203 REF		
b	0.15	0.2	0.25
D	5 BSC		
E	5 BSC		
e	0.4 BSC		
J	3.5	3.6	3.7
K	3.5	3.6	3.7
L	0.35	0.4	0.45